ASSIGNMENT 6

Textbook Assignment: "Central Processing Units and Buses," chapter 5—continued, pages 5-24 through 5-29; "Computer Memories," chapter 6, pages 6-1 through 6-20.

6-1. The buses in a computer are controlled by (a) what functional area and (b) what type of communication path is used?

1. (a) CPU (b) serial
2. (a) CPU (b) parallel
3. (a) Memory (b) serial
4. (a) Memory (b) parallel

6-2. All the following types of information are transferred over buses except which type?

1. Power
2. Data
3. Commands
4. Instructions

6-3. The preferred method of transfer for data/information between system components is which of the following?

1. Control bus
2. Common data bus
3. Operand bus
4. Address bus

6-4. What IEEE standard is used for a simple 32-bit backplane bus?

1. 1196
2. 1296
3. 896.1
4. 1014

A. Control bus
B. Address bus
C. Data bus
D. Instruction (I) bus
E. Operand (C) bus
F. I/O mem bus or IOC bus
G. Time multiplexed bus
H. DMI bus

Figure 6-A.—Buses.

IN ANSWERING QUESTIONS 6-5 THROUGH 6-11, REFER TO FIGURE 6-A. SELECT THE NAME(S) OF THE BUS OR BUSES THAT IS/ARE DESCRIBED IN EACH QUESTION.

6-5. This bus has all the signals necessary to define any of the possible memory address locations within the computer or a module.

1. A
2. B
3. C
4. D

6-6. This bus (or buses) can be used to transfer instructions from memory to the CPU.

1. A
2. B
3. C only
4. Both C and D

6-7. This bus allows communication between the CPU and memory or the CPU and the IOC.

1. C
2. D
3. E
4. F

6-8. Controlled by the IOC, this bus responds to the CPU by using the O bus.

1. E
2. F
3. G
4. H

6-9. This bus transmits individual signals to control and coordinate the operations of the computer.

1. A
2. B
3. C
4. D

6-10. This bus transmits addresses and data by using clock cycles.

1. E
2. F
3. G
4. H

6-11. Acts as a requester, this bus is used to send requests from other computers.

1. E
2. F
3. G
4. H

6-12. What device accepts requests and uses a priority network to determine the order in which it is to respond to the requesters?

1. Operand bus extender
2. REI bus extender
3. CPU
4. DMI

6-13. Regardless of whether a computer has an IOC or not, the CPU will control all buses.

1. True
2. False

6-14. In bus communications, which of the following factors relating to the data being transferred must be considered?

1. Source only
2. Destination only
3. Transfer priority only
4. Source, destination, and transfer priority

6-15. Bus requests may be made by all of the following parts except which one?

1. CPU
2. IOC
3. Memory
4. DMI

6-16. Holding registers are used by source and destination sections to prevent data loss and to help coordinate data exchange.

1. True
2. False

6-17. In the exchange of data on the buses, (a) what logic generates a ready signal when data is in the holding register and on the bus and (b) what logic sends an accept signal?

1. (a) Source (b) source
2. (a) Source (b) destination
3. (a) Destination (b) source
4. (a) Destination (b) destination

6-18. Which of the following items is stored in main memory?

1. Data and programs only
2. Calculations and operands only
3. Data, programs, and PROMS
4. Data, programs, calculations, and operands

A. Memory address
B. Capacity
C. Access time
D. Destructive readout
E. Non-destructive readout
F. Volatile memory
G. Nonvolatile memory

Figure 6-B.—Terminology.

IN ANSWERING QUESTIONS 6-19 THROUGH 6-24, REFER TO FIGURE 6-B. SELECT THE TERM THAT MATCHES THE DESCRIPTION IN EACH QUESTION.

6-19. Time interval from the instant a request for data is initiated until the data is available for use.

1. A
2. B
3. C
4. D

6-20. The output side of a flip-flop is read from memory without having to be rewritten.

1. D
2. E
3. F
4. G

6-21. The power to the computer is turned off and the contents of memory are retained.

1. D
2. E
3. F
4. G

6-22. The particular location of a larger memory array where a packet of information is located.

1. A
2. B
3. C
4. D

6-23. Power is shut off to the computer and the contents of the semi- conductor memory are lost.

1. D
2. E
3. F
4. G

6-24. The data is lost when it is read from memory.

1. A
2. B
3. C
4. D

6-25. A memory unit that can receive requests from more than one CPU or I/O section is known as which of the following types of memories?

1. Memory pcb
2. Single-inline memory module
3. Multiported memory module
4. Dual-action memory module

6-26. Pcb type memories are usually composed of which of the following memory types?

1. Semiconductor
2. Core
3. Film
4. Both 2 and 3 above

6-27. In a typical square form memory, the intersection of an x row and y column is called a

1. memory word address
2. memory word
3. memory module
4. memory cell

6-28. The x rows and y columns of a typical memory will be equal in number.

1. True
2. False

6-29. Memory operations in most computers usually include which of the following items?

1. Control circuits
2. Timing circuits
3. Memory cycle
4. All of the above

6-30. Memory interface circuits include which of the following items?

1. Address register
2. Communication lines
3. Interfacing register
4. Both 2 and 3 above

6-31. A word is read from memory, then rerouted back through the Z register to be rewritten. This is what type of memory?

1. Non-destructive readout
2. Destructive readout
3. Hardwired
4. ROM

6-32. Priority of memory requests are evaluated by which of the following devices?

1. Control circuits
2. Address register
3. Z register
4. CPU

6-33. Memory read/write enables are provided by which of the following devices?

1. Control circuits
2. Timing circuits
3. CPU
4. I/O control

6-34. During a complete memory cycle, the first thing that must occur is which of the following?

1. Registers used for read/write operations are cleared
2. Enables are generated to gate memory address into registers used for read/write operations
3. Memory address translation is accomplished
4. Interface logic acknowledges reading data from memory

6-35. To locate a memory address word, the computer uses which of the following items in memory?

1. Timing circuits
2. Control circuits
3. Interface circuits
4. Memory logic

6-36. The conversion from a logical to a physical memory address is a function of which of the following items in memory?

1. Memory logic
2. Timing circuits
3. Control circuits
4. Interface circuits

6-37. In all computers, for every read operation there will always be a corresponding write operation.

1. True
2. False

6-38. In order to increase memory speed using interleaving, which of the following items are required?

1. Memory modules of 32 bits
2. A minimum of 8 memory modules
3. More complex CPU and memory control circuitry
4. All of the above

6-39. When odd parity is used for memory fault detection, all words stored in memory will have which of the following bits?

1. A logic 1 parity bit
2. A logic 0 parity bit
3. An even number of set bits stored at each memory location
4. An odd number of set bits stored at each memory location

6-40. The memory protection register set is used for which of the following purposes?

1. To restrict read/write operations in portions of memory
2. To protect memory from unplanned power loss
3. To protect against erroneous write instructions
4. To limit access of memory to authorized users

6-41. In a memory segment within the protected area with all three bits of the memory protection control register set, which of the following operations are allowed?

1. Execute protected
2. Write protected
3. Read protected
4. All of the above

6-42. Memory lockout is used by larger computers to prevent access to particular areas of memory by task state instructions. Which of the following describes the lockout function?

1. It is disabled when the CPU enters a particular executive or interrupt state and enabled when the CPU enters the task state
2. It is enabled when the CPU enters a particular executive or interrupt state and enabled when the CPU enters the task state
3. It is enabled when the CPU enters a particular executive ‘or interrupt state and disabled when the CPU enters the task state
4. It is disabled when the CPU enters a particular executive or interrupt state and disabled when the CPU enters the task state

6-43. Compared with semiconductor memories, magnetic memories have which of the following advantages?

1. They cost less
2. They are faster in terms of storage and access
3. They require less power and they are volatile
4. They require less power and they are nonvolatile

6-44. The state of a core or film is changed by which of the following conditions?

1. Current flow in the opposite direction of sufficient magnitude to overcome the magnetic field and to magnetize in the new direction
2. Current flow in the same direction of sufficient magnitude to match the magnetic field and to magnetize in the old direction
3. Voltage amplitude of a sufficient magnitude to overcome the magnetic field and to magnetize in the new direction
4. Current flow in the opposite direction of sufficient magnitude to overcome the magnetic field and to magnetize in the old direction

6-45. Compared with core memory, film memory has which of the following advantages?

1. Increased speed of read/write operations and less power required
2. More compact and durable
3. Twice as many memory cells can be put in the same space for the same amount of power
4. Each of the above

6-46. Each ferrite core can store what total number of bits?

1. One
2. Two
3. Three
4. Four

6-47. In a four-wire core winding, what is the physical make up of the windings that are strung through each and every core?

1. 1 drive line, 1 sense line, and 1 inhibit line
2. 2 drive lines, 1 sense line, and 2 inhibit lines
3. 2 drives lines, 1 sense line, and 1 inhibit line
4. 2 drive lines, 2 sense lines, and 1 inhibit line

IN ANSWERING QUESTIONS 6-48 THROUGH 6-51, SELECT THE CORE LINE THAT MATCHES THE DESCRIPTION IN EACH QUESTION.

1. Drive line
2. Sense line
3. Inhibit line

6-48. Detects the change in state of the core from one to zero.

6-49. Each line provides 1/2 of the current necessary to change the state of the core.

6-50. Prevents changing the core from a zero to a one.

6-51. In a three-wire core, this line performs the same function as in the four-wire core.

6-52. To simplify addressing, reading, and writing operations, magnetic cores are arranged in which of the following ways?

1. In hierarchical patterns
2. In matrices
3. In planes
4. In stacks

6-53. Which core in an array will be switched from one state to another?

1. A core with a full read or write current passing through it
2. A core with a half read current passing through it
3. A core with a half write current passing through it
4. A core with a half read or write passing through it

6-54. In a core array the inhibit line is threaded in ____(a)____ with the x or y drives
(series, parallel)
lines and the sense line threaded through _____(b)____ core.
(each, every other)

1. (a) Series (b) each
2. (a) Parallel (b) each
3. (a) Series (b) every other
4. (a) Parallel (b) every other

6-55. What is the basic building block of the memory stack?

1. Matrix
2. Array
3. Plane
4. Quadrant

6-56. The address register bits are used to translate the bits to make which of the following bit selections?

1. Stack only
2. Inhibit upper and lower stack only
3. X and Y primary, secondary, and diode only
4. X and Y primary, secondary, and diode; stack; and inhibit upper and lower stack

6-57. Which selectors are activated only when writing zeros?

1. Inhibit
2. X and Y primary
3. X and Y secondary
4. X and Y read/write diode

6-58. In a core read/write cycle, the read current is designed to change the state of the core(s) to (a) what value; and the write current is designed to change the state of the core(s) from (b) what value to (c) what value?

1. (a) Zero (b) zero (c) one
2. (a) Zero (b) one (c) one
3. (a) One (b) zero (c) one
4. (a) One (b) one (c) one

6-59. The process of reading cores to the zero state is known as which of the following types of readout?

1. Destructive readout
2. Non-destructive readout
3. Volatile readout
4. Nonvolatile readout

6-60. In a core memory, a restore cycle is necessary after data has been read from memory for what reason, if any?

1. To change the state of each selected core from zero to one
2. To change the state of all the cores from one to zero
3. To sense the state of each core
4. None, a restore cycle is not needed

6-61. During a restore operation of zeros in a three-wire core, the absence of write current on which of the following lines will leave the cores in the zero state?

1. Digit
2. Word
3. X drive
4. Y drive

6-62. What specific number of paired film spots is used for each bit position?

1. One
2. Two
3. Three
4. Four

6-63. Current flow through which of the following lines will magnetize a film spot?

1. Drive
2. Word only
3. Sense/digit only
4. Word or sense/digit, depending on the function

6-64. In the application of external fields, the longitudinal fields are produced by passing the current (a) in which of the following ways and the transverse fields are produced by passing the current (b) in which of the following ways?

1. (a) Down the word line
   (b) In the proper direction along the sense/digit line
2. (a) In the proper direction along the word line
   (b) Down the sense/digit line
3. (a) In the proper direction along the sense/digit line
   (b) Down the word line
4. (a) In the proper direction along the sense/digit line
   (b) Down the drive line

6-65. In a film memory, a packet stores what specific number of bits of data?

1. One
2. Two
3. Three
4. Four

6-66. Which, if any, of the following devices makes the mated film cells less susceptible to the disturbance from other cells in close proximity to them?

1. Ground plane
2. Insulator
3. Keeper
4. None of the above

6-67. How is mated film memory structured?

1. Bit organized
2. Stack organized
3. Word organized
4. Array organized

6-68. What item is the basic building block of the film memory stack?

1. Matrix
2. Array
3. Packet
4. Plane

6-69. The memory capacity of a film core storage device is determined by which of the following factors?

1. Size of the computer
2. Number of packets only
3. Size of the array in the memory stack only
4. Number of packets and the size of the array in the memory stack

6-70. In film storage, up to how many words can be selected at each memory location?

1. One
2. Two
3. Three
4. Four

6-71. The address register bits used to translate the bits to make selections are processed in which of the following sequences?

1. Word at the address location, memory location, and stack
2. Stack, word at the address location, memory location
3. Word at the address location, stack, and memory location
4. Stack, memory location, and word at the address location

6-72. A mated film memory cell is read by which of the following methods?

1. A current is generated along the digit line and a transverse field is applied to the thin film cell
2. A current is generated along the sense line and a transverse field is applied to the thin film cell
3. A current is generated along the word line and a transverse field is applied to the thin film cell
4. A current is generated along the word line and a longitudinal field is applied to the thin film cell

6-73. What factor will determine the recorded state of the film?

1. The direction of the cell vector rotation induced film signal on the sense/digit line
2. The direction of the cell vector rotation induced film signal on the word line
3. The magnitude of the cell vector rotation induced film signal on the digit line
4. The direction of the cell vector rotation induced film signal on the sense line

6-74. When a one is to be stored, (a) what is the direction of the bit current in relationship to that used to store a zero and (b) what field steers the vector to the one state?

1. (a) The same
   (b) Transverse
2. (a) The same
   (b) Longitudinal
3. (a) Reversed
   (b) Transverse
4. (a) Reversed
   (b) Longitudinal

6-75. In a restore operation of a film memory, what factor determines the direction of the digit current on the sense/digit line?

1. Binary value of the data register
2. Direction of current on the word line
3. The easy axis
4. The hard axis